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			Application Number	Not Yet Assigned	
			Filing Date	On Even Date Herewith	
			First Named Inventor	K. ISHIBASHI, et al.	
			Art Unit	Not Yet Assigned	
Examiner Name	Not Yet Assigned				
Attorney Docket Number	520.39604CX1				
Sheet	1	of	1		

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
SP		US-	5,485,231	11-1995	Ohsaki	
SP		US-	5,457,335	10-1995	Kuroda et al.	
SP		US-	5,163,023	11-1992	Ferris et al.	
SP		US-	5,089,433	02-1992	Anand et al.	
SP		US-	4,784,597	12-1988	Ooba et al.	
SP		US-	6,115,293	09-2000	M. Yamashita	
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		US-				

FOREIGN PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ² -Number ¹ -Kind Code ² (if known)				
SA		JP 7287894	10-1995			
SA		JP 785892	03-1995			
SA		JP 60201589	10-1985			
SA		JP 61123100	08-1988			
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SA		JP 5114300	05-1993			
SA		JP 10149894	08-1998			
SA		JP 5314789	11-1993			
SA		1197652	01-1999			

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS			
Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
SP		Takai et al., "A 250Mv/s/pin 1Gb Double Data Rate SDRAM with a Bi-Directional Delay and an Inter-Bank Shared Redundancy Scheme", 1999 IEEE Int'l Solid-State Circuits Conference, pp. 418-419	

Examiner Signature		Date Considered	11/1/04
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